

103

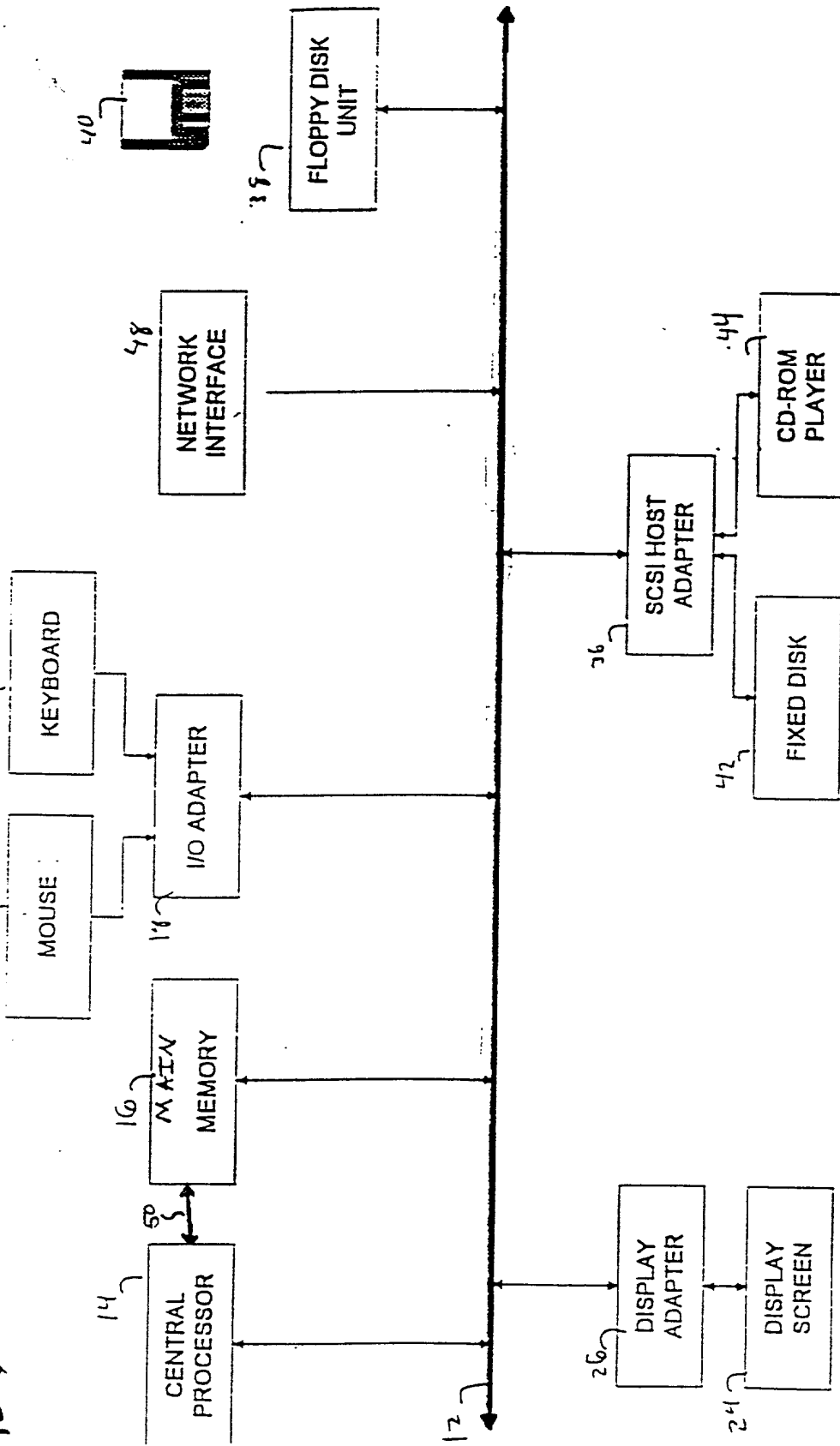


Fig. 1A
(Prior Art)

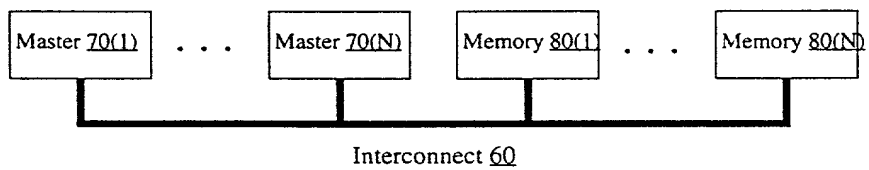


Fig. 1B

(>not int)

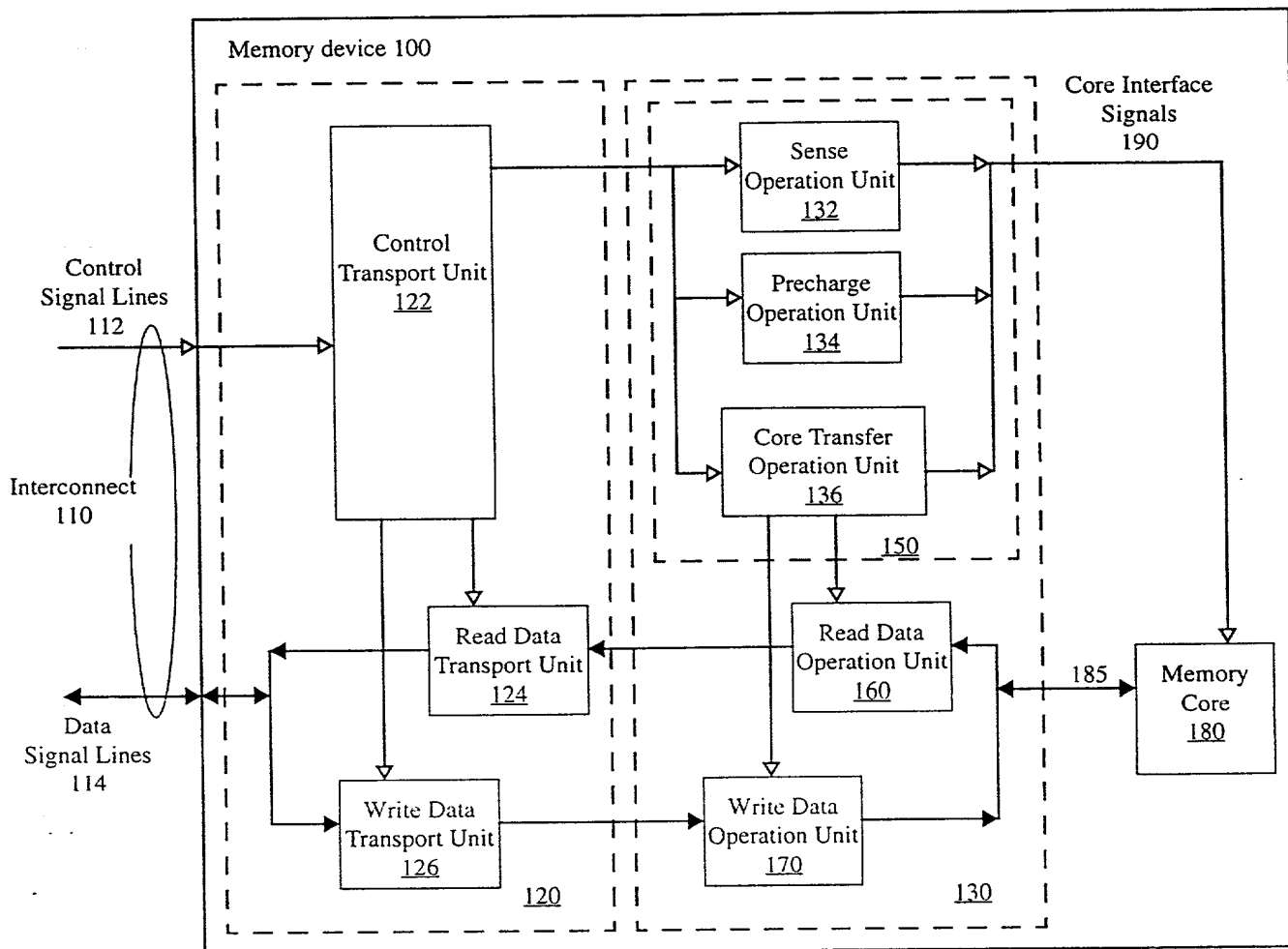


Fig. 1C
(Prior Art)

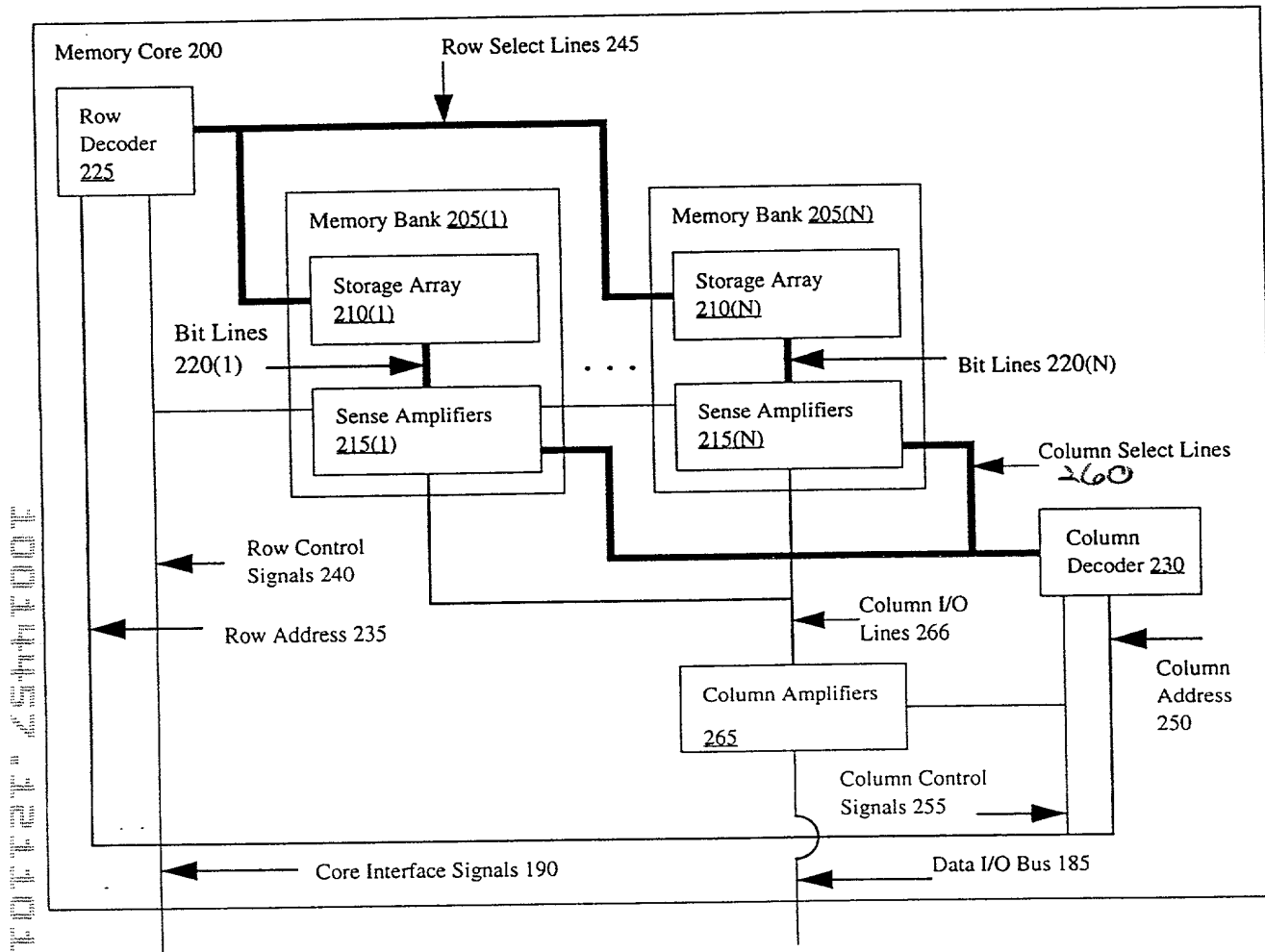


Fig. 2

(Prior Art)

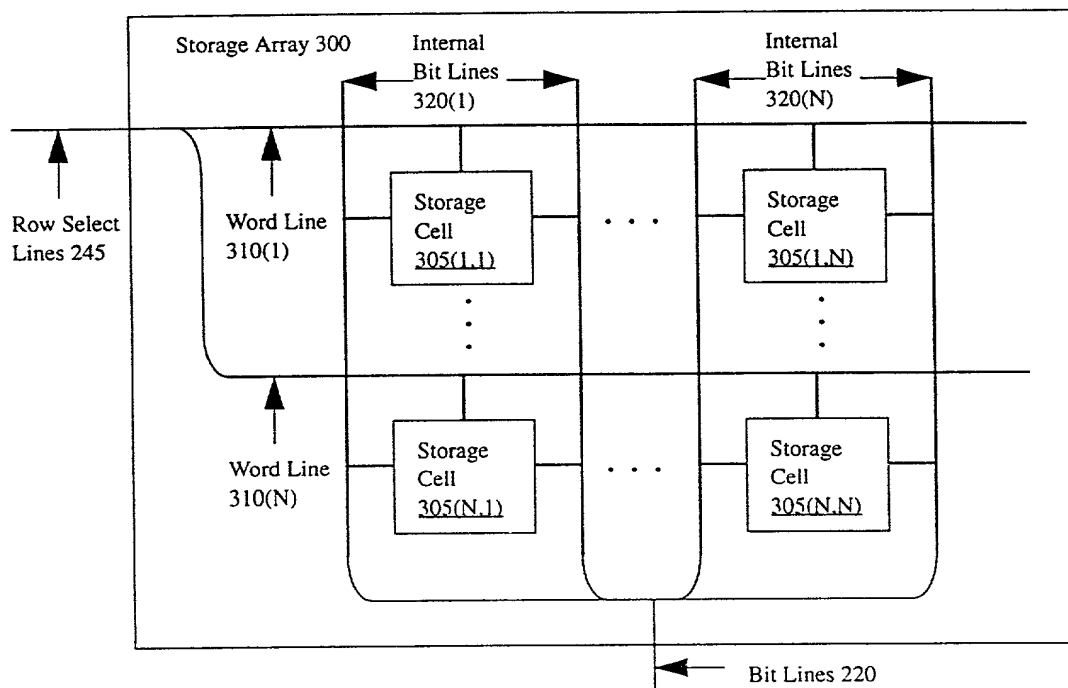


Fig. 3
(Prior Art)

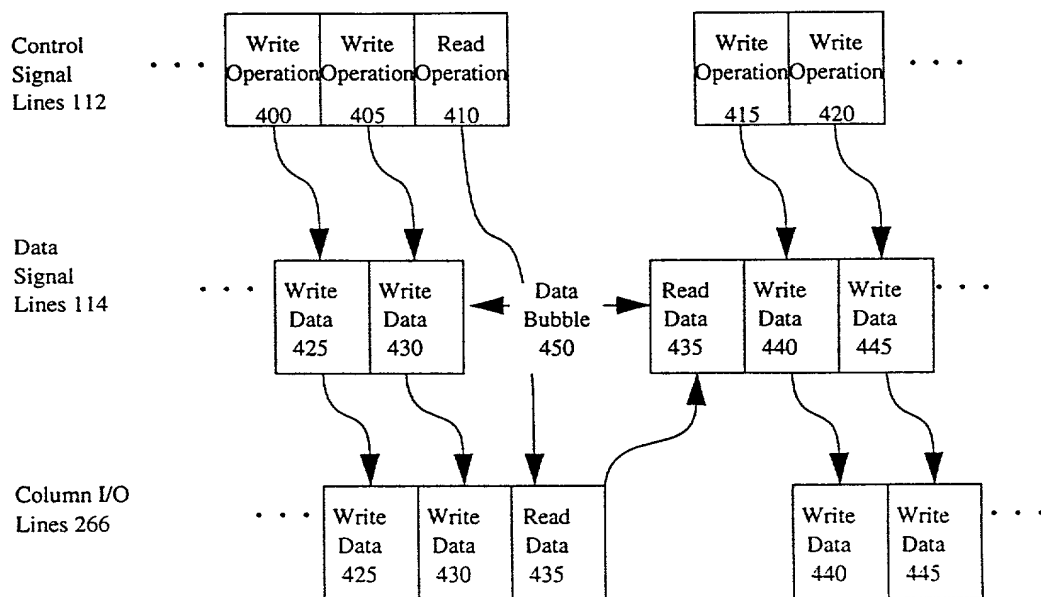


Fig. 4

(Prior art)

Control
Signal
Lines 112

Data
Signal
Lines 114

Column I/O Lines 266
(Device A)

Column I/O Lines 266
(Device B)

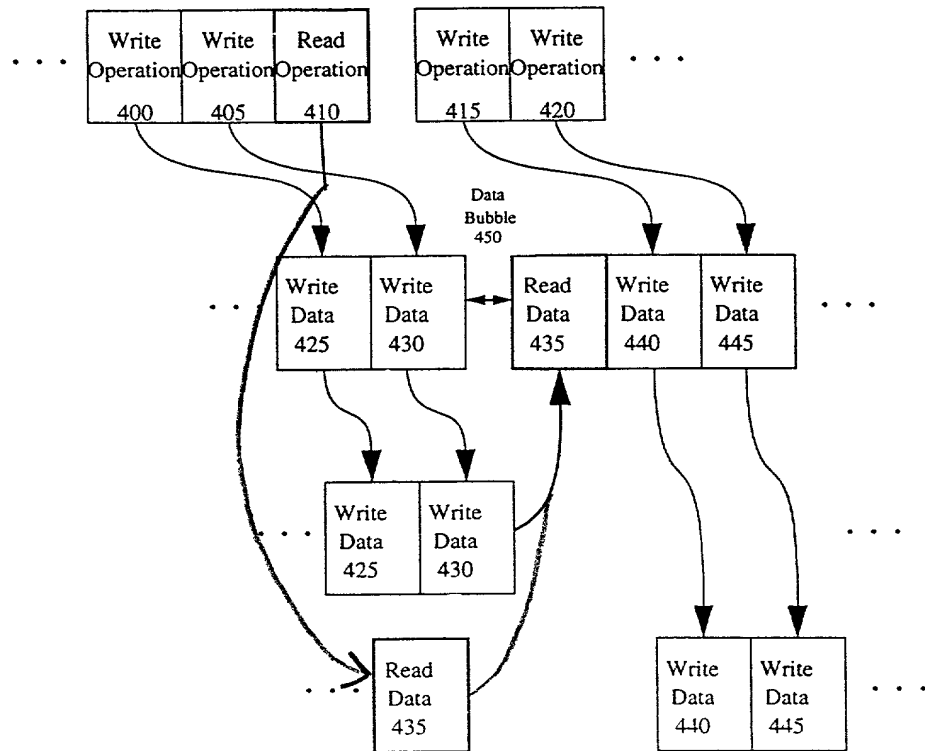


Fig. 5

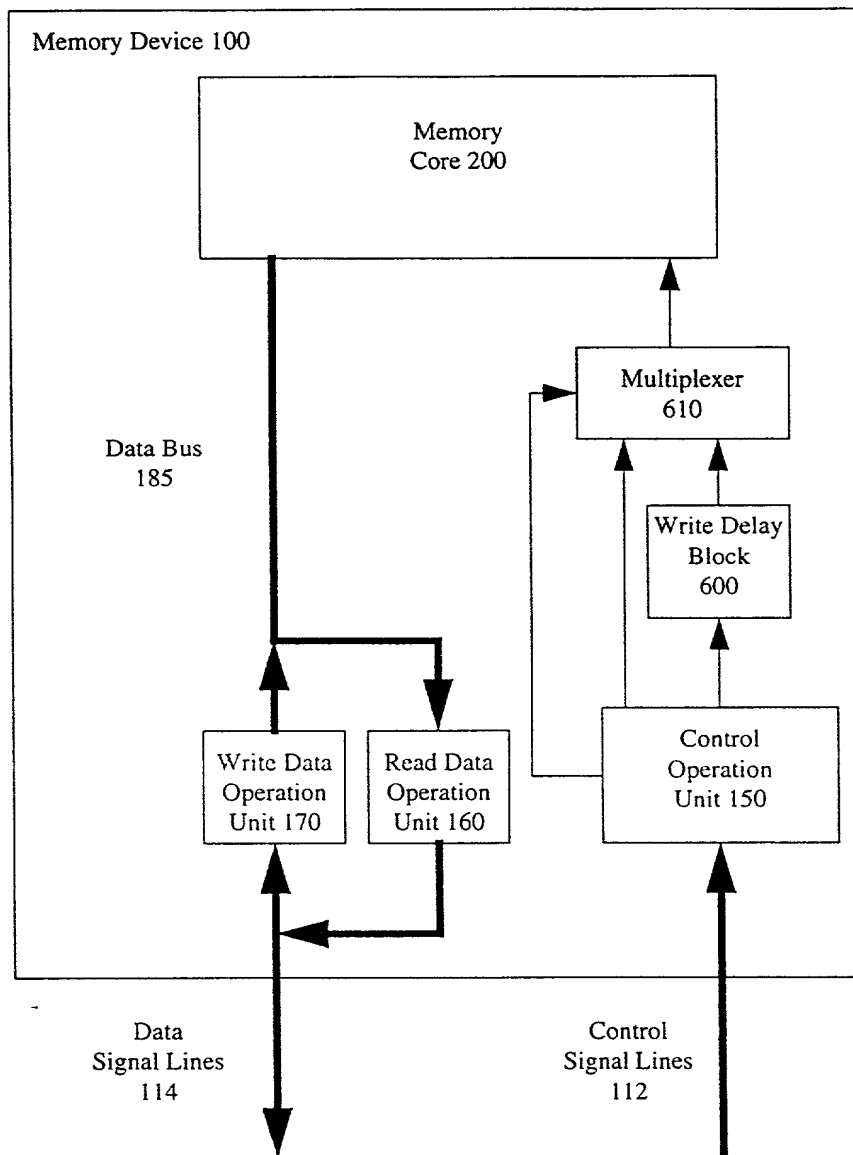


Fig. 6

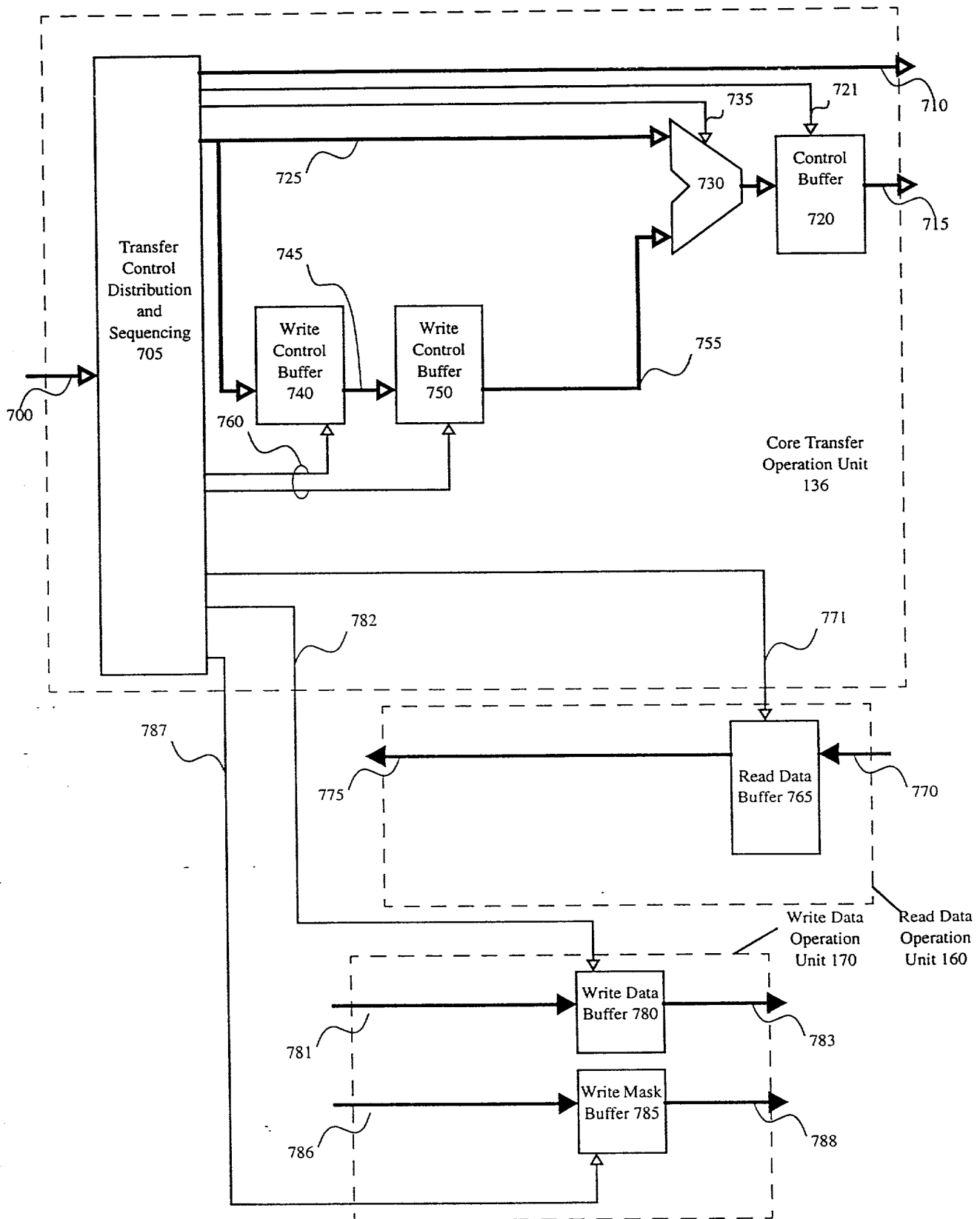


Fig. 7

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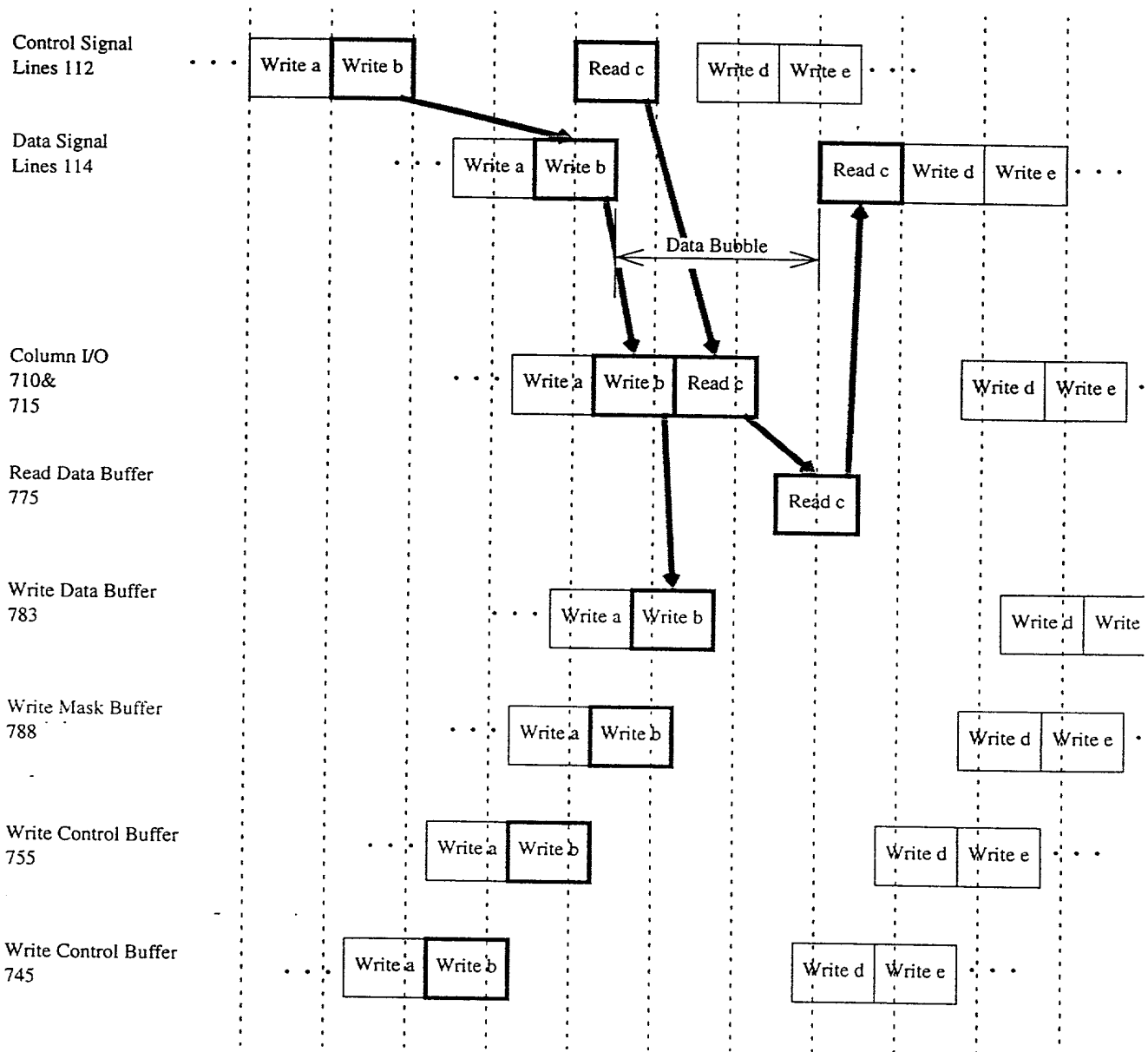


Fig. 8

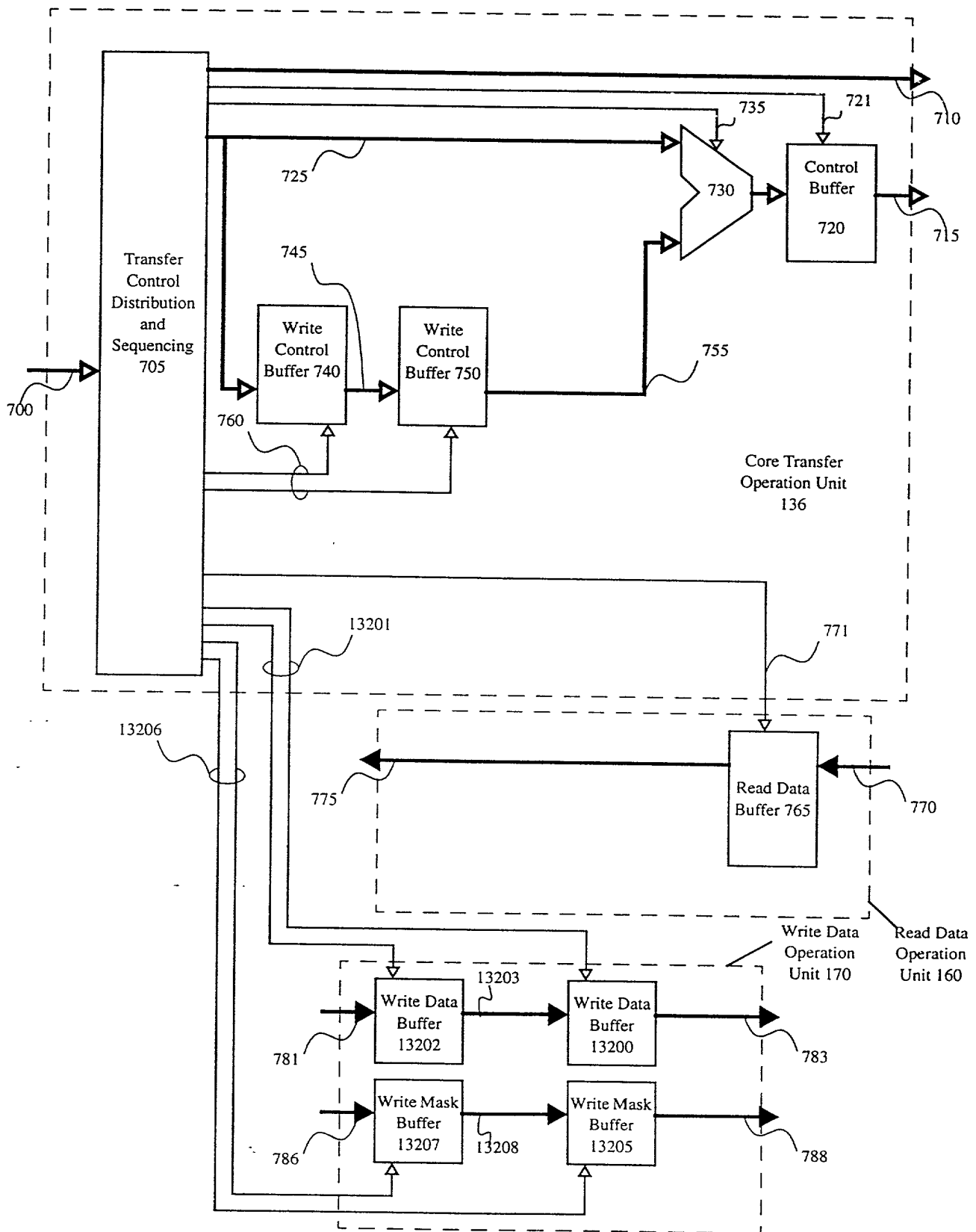


Fig. 9

Control Signal
Lines 112

Data Signal
Lines 114

Column I/O
710&
715

Read Data Buffer
775

Write Data Buffer
783

Write Data Buffer
13203

Write Mask Buffer
788

Write Mask Buffer
13208

Write Control Buffer
755

Write Control Buffer
745

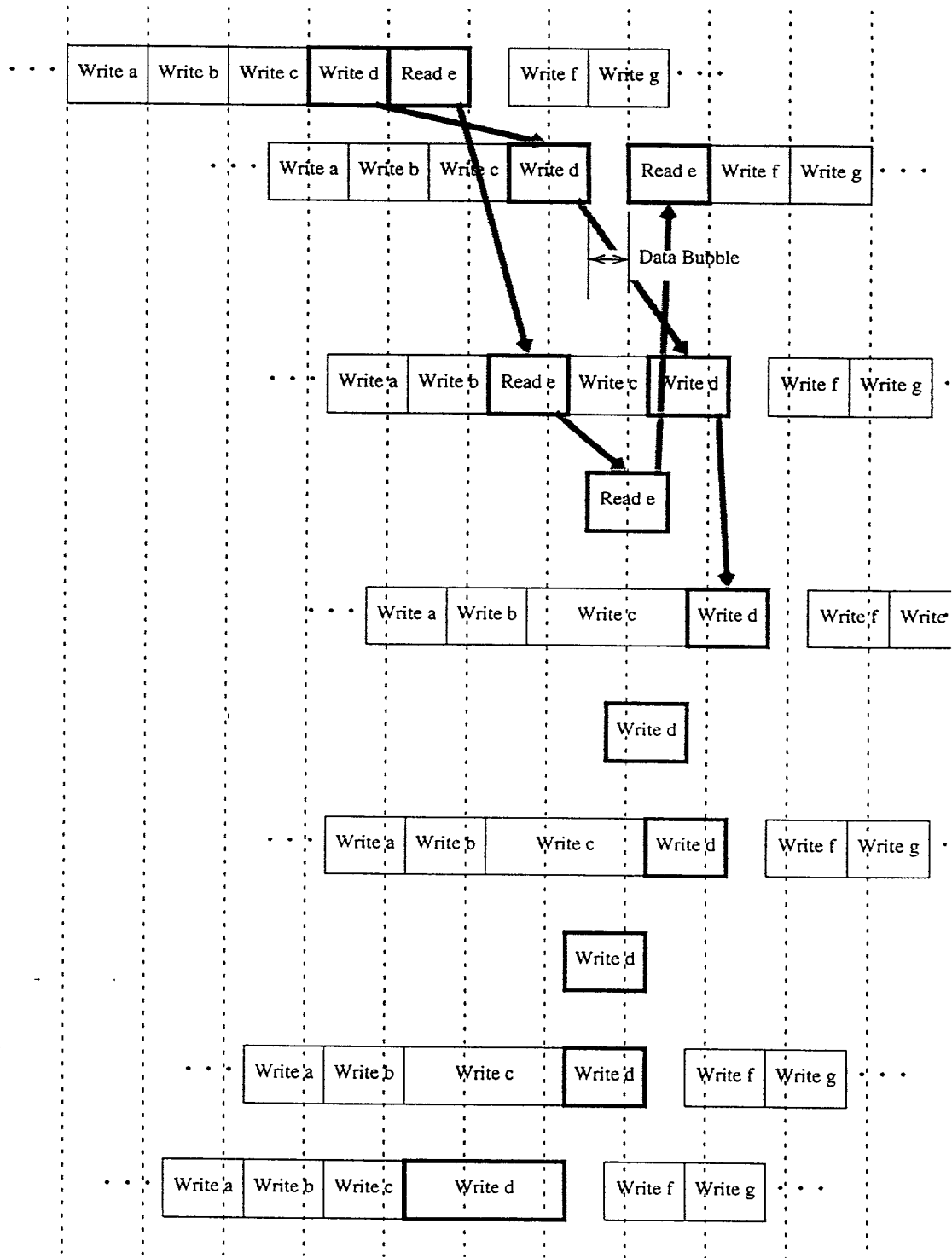


Fig. 10

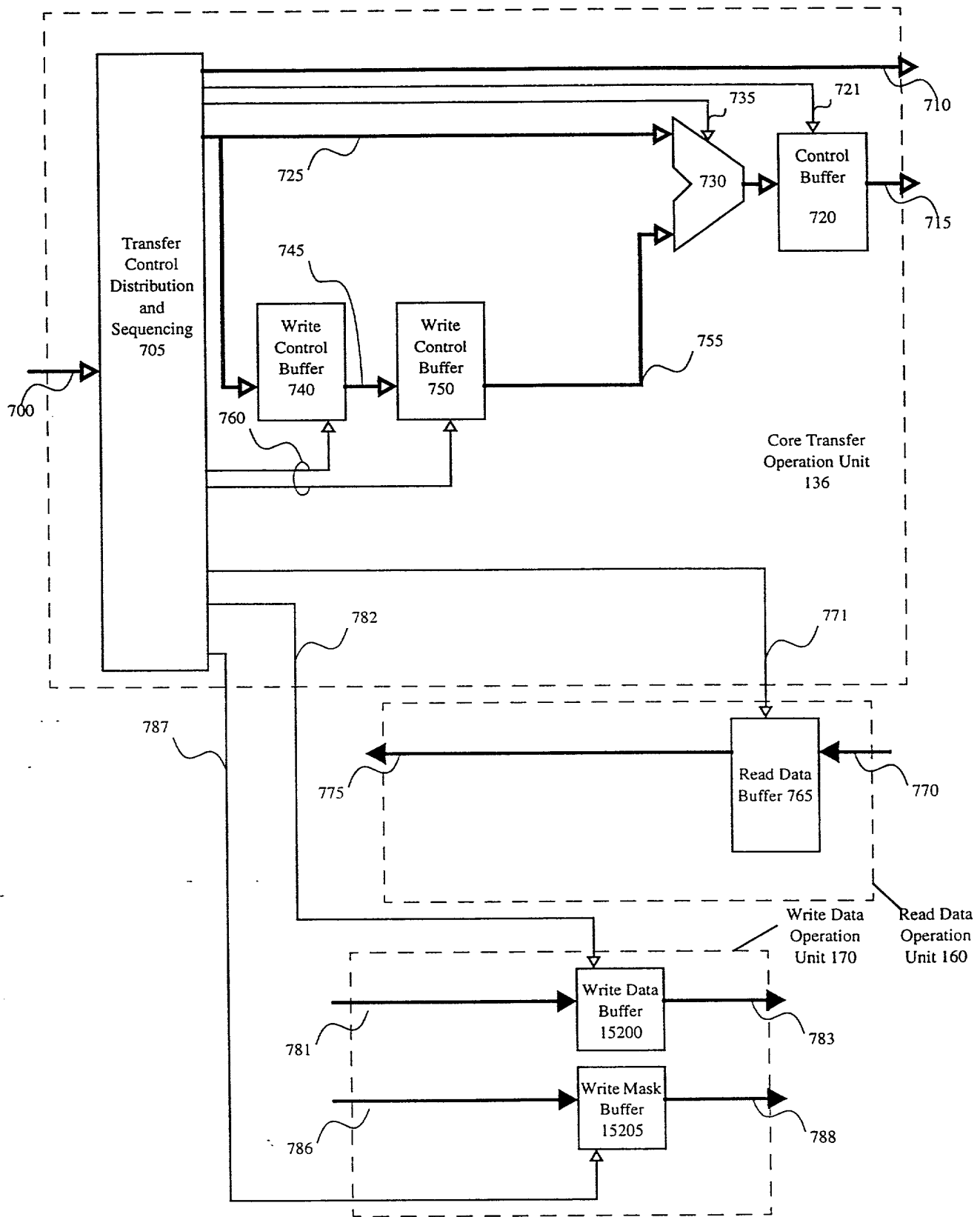


Fig. 11

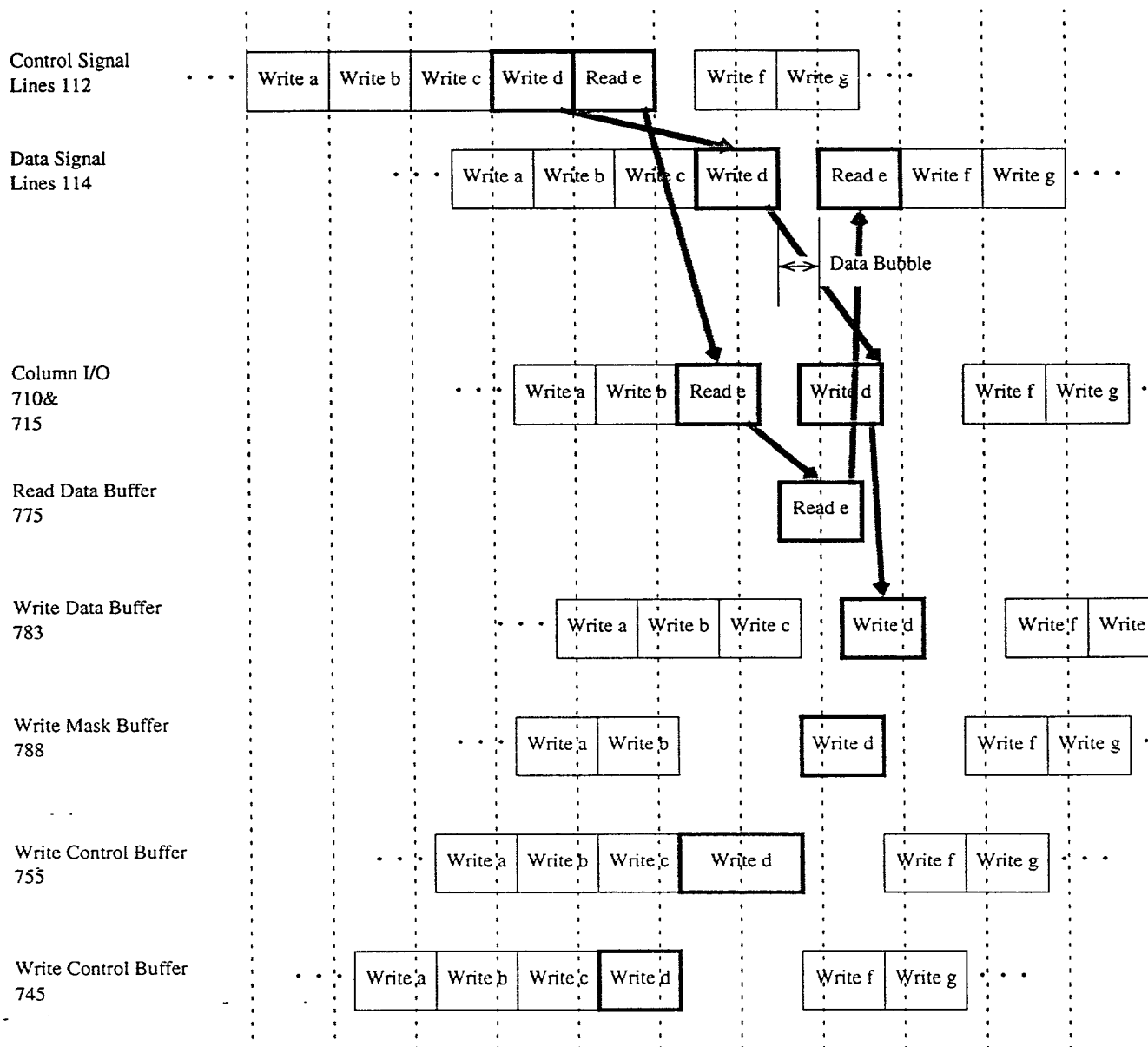


Fig. 12

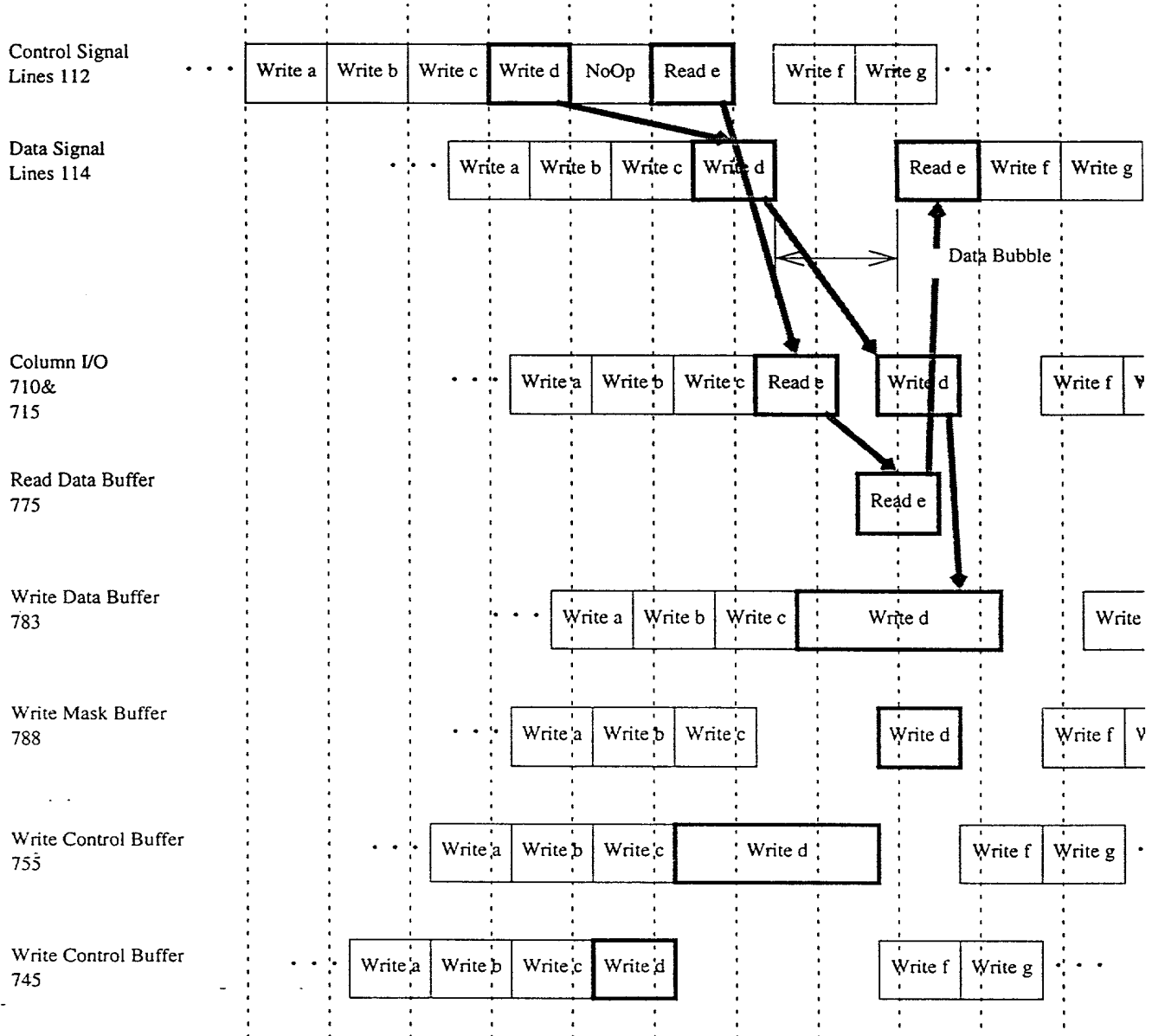


Fig. 13

Control Signal
Lines 112

Data Signal
Lines 114

Column I/O
710 &
715

Read Data Buffer
775

Write Data Buffer
783

Write Mask Buffer
788

Write Control Buffer
755

Write Control Buffer
745

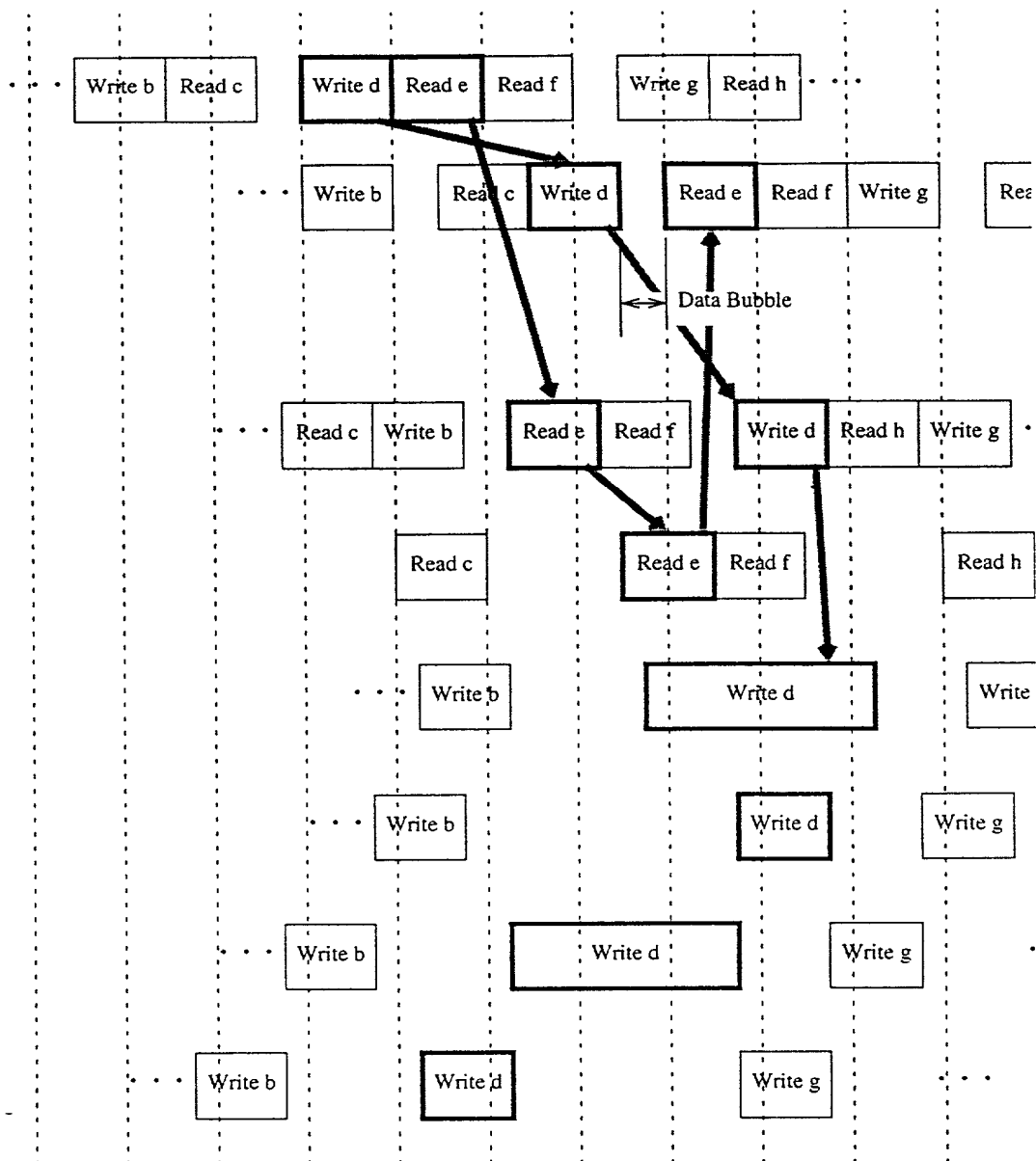


Fig. 14

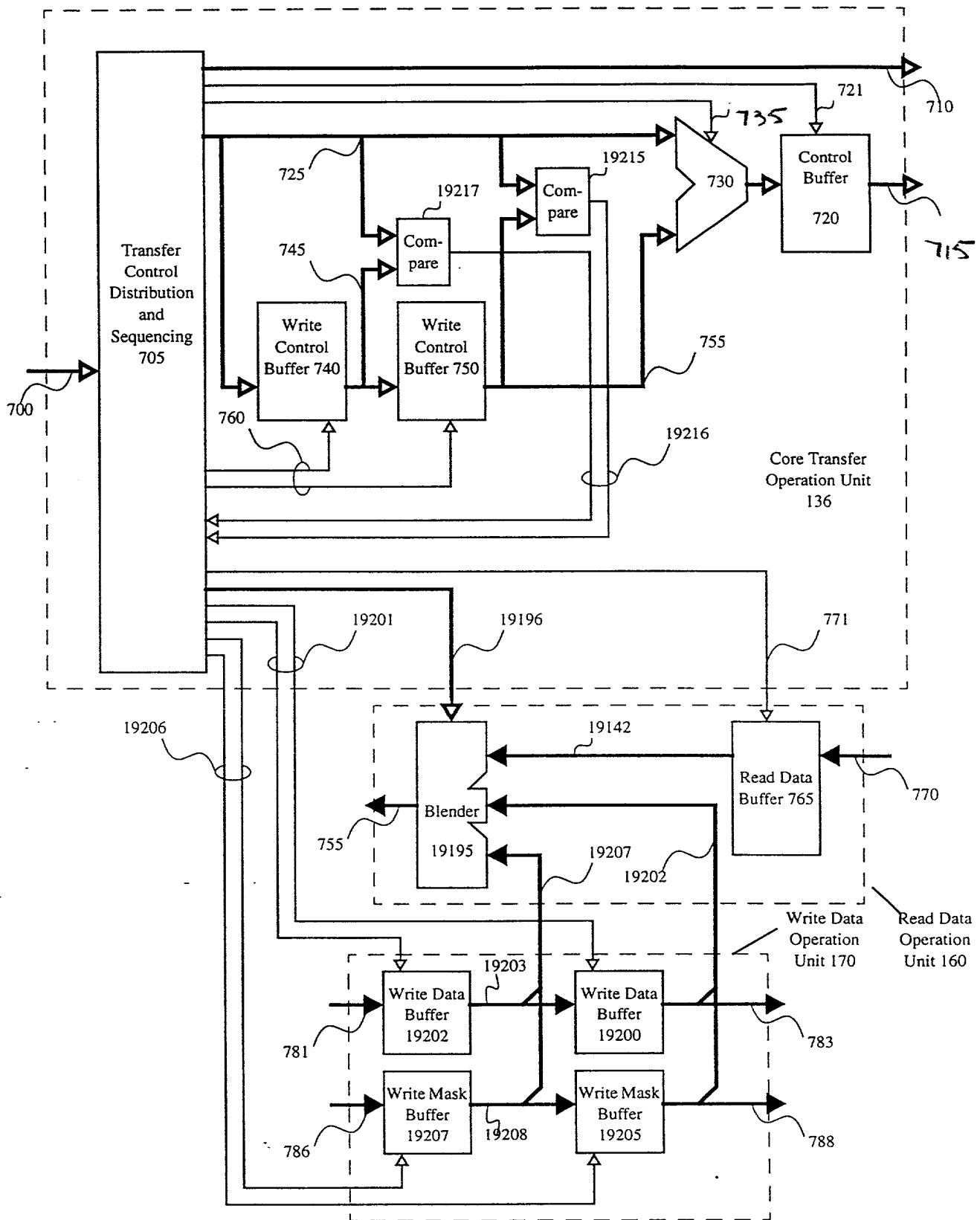


Fig. 15

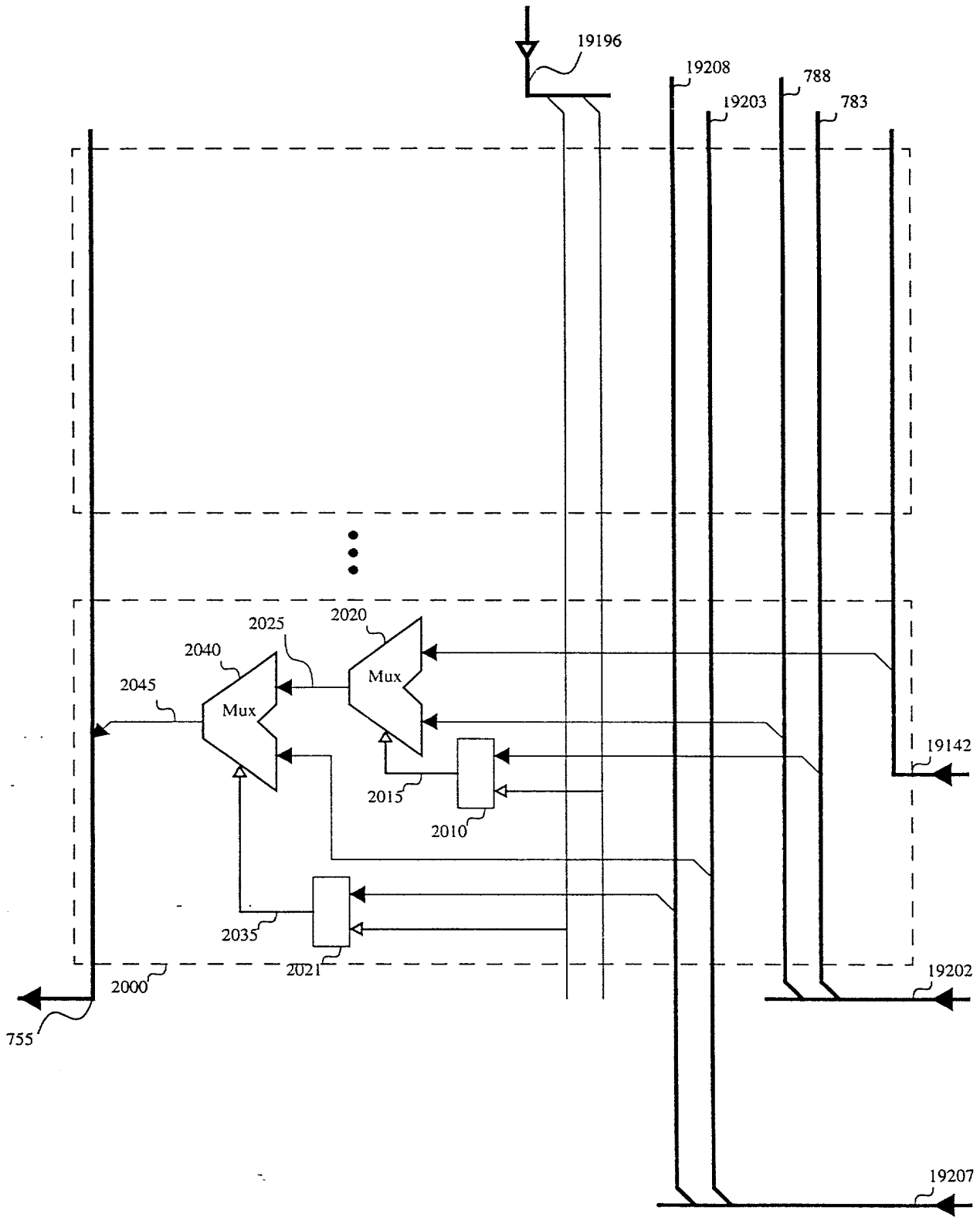


Fig. 16

Fig. 17

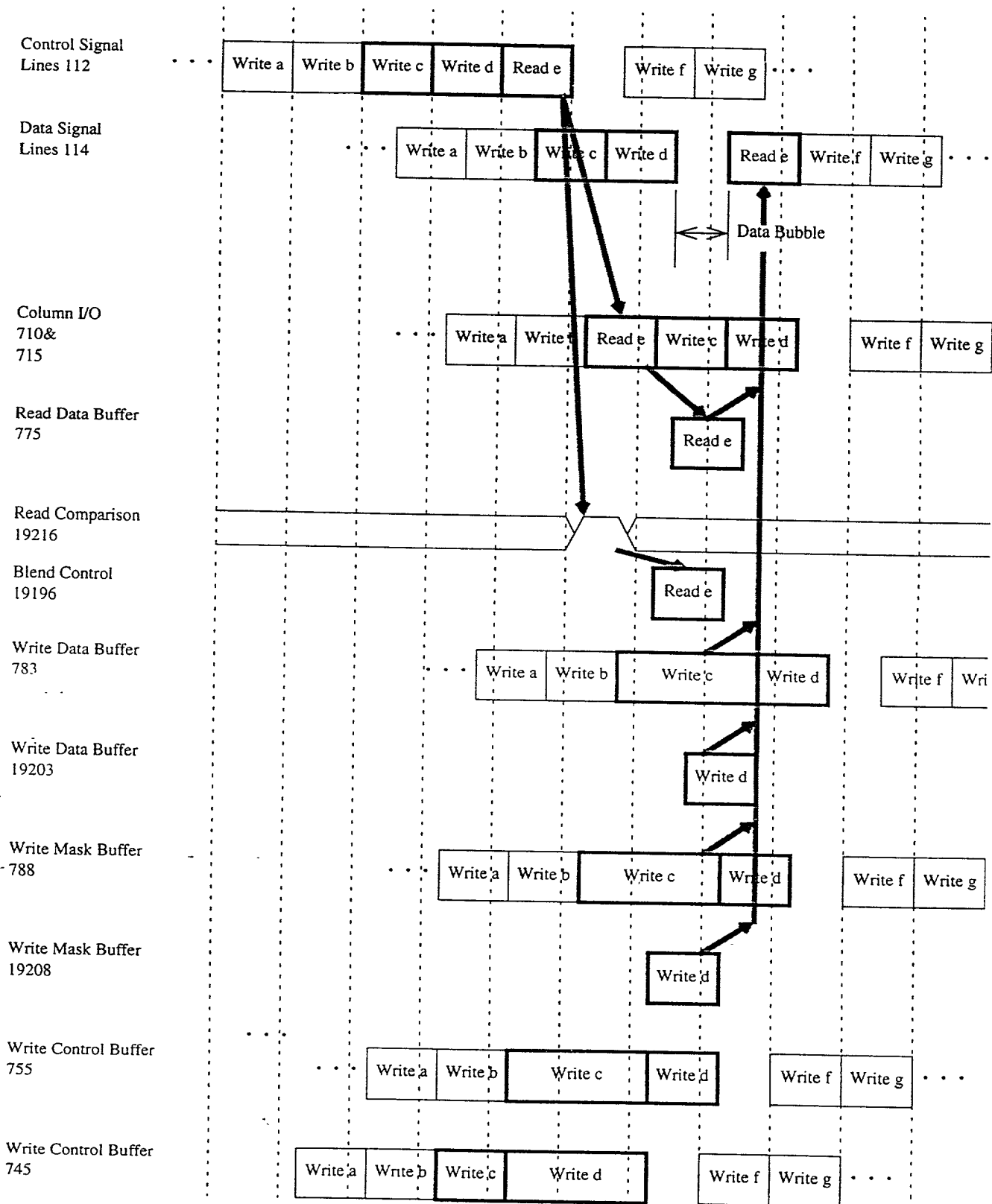


Fig. 18